REMARKS

In the Official Action mailed on **30 January 2006**, the Examiner reviewed claims 1-25. Claims 1-3, 5-15, and 17-25 were rejected under 35 U.S.C. 102(b) as being anticipated by Moss et al. (*"Transactional Memory: Architectural Support for Lock-Free Data Structures"* hereinafter "Moss"). Claims 4 and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Moss, in view of Oplinger et al. (*"Enhancing Software Reliability with Speculative Threads"* hereinafter "Oplinger").

Rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a)

Claims 1, 13, and 25 were rejected under 35 U.S.C. §102(b) as being anticipated by Moss et al. (*"Transactional Memory: Architectural Support for Lock-Free Data Structures"* hereinafter "Moss").

Applicant respectfully points out that the ABORT instruction taught in Moss **causes the hardware to discard all updates to the write set** (see Moss, section 2.1). In other words, Moss discloses a system wherein an ABORT instruction is only used to discard the results of transactional execution upon encountering certain conditions, such as interrupts, context switches, or in the event of a serialization conflict (see Moss, section 2.1).

In contrast, the FAIL instruction in the present invention also provides the processor with the ability to **branch to a location in the program code specified by a branch target field of the FAIL instruction** (see FIG. 9, element 920, and page 20, lines 11-17 of the instant application). Consequently, the programmer can use the FAIL instruction to **branch to an error handler or code that performs other operations** in addition to mechanically discarding transactional updates (see page 20, lines 11-22 of the instant application). Providing the FAIL instruction with this capability is beneficial because a programmer has

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significantly more control over the operation of the processor while terminating transactional execution.

Accordingly, Applicant has amended independent claims 1, 13, and 25 to include the limitations in dependent claim 5 which specify that the FAIL instruction may branch to other locations in the program code. These amendments find support in page 20, lines 11-22 of the instant application. Claims 5 and 17 have been cancelled without prejudice.
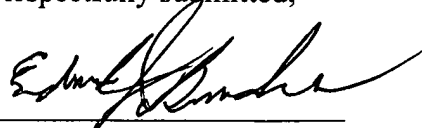
Hence, Applicant respectfully submits that independent claims 1, 13, and 25 as presently amended are in condition for allowance. Applicant also submits that claims 2-4 and 6-12, which depend upon claim 1, and claims 14-16 and 18-24, which depend upon claim 13, are in condition for allowance for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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